

FIG.1

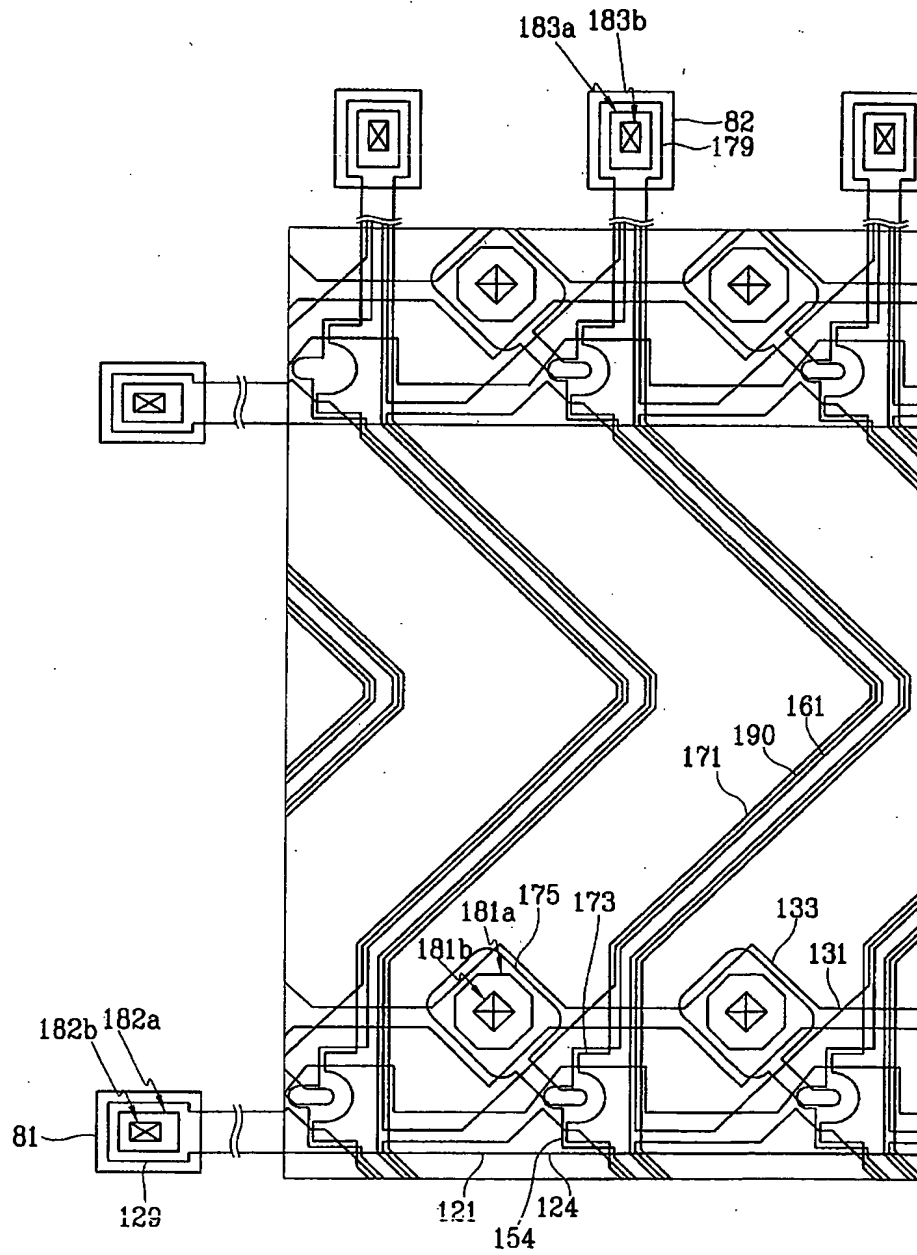


FIG.2

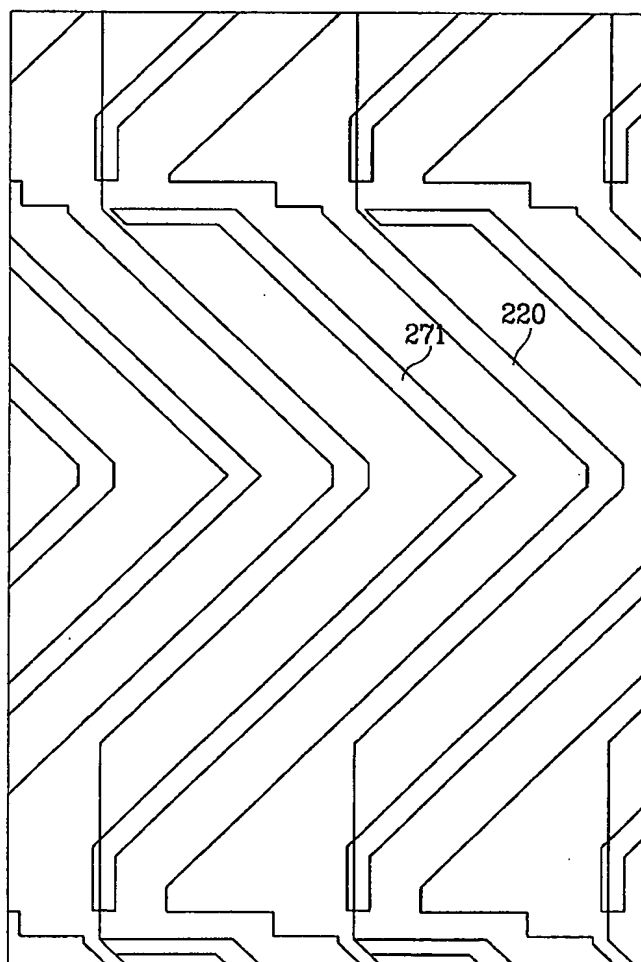


FIG.3

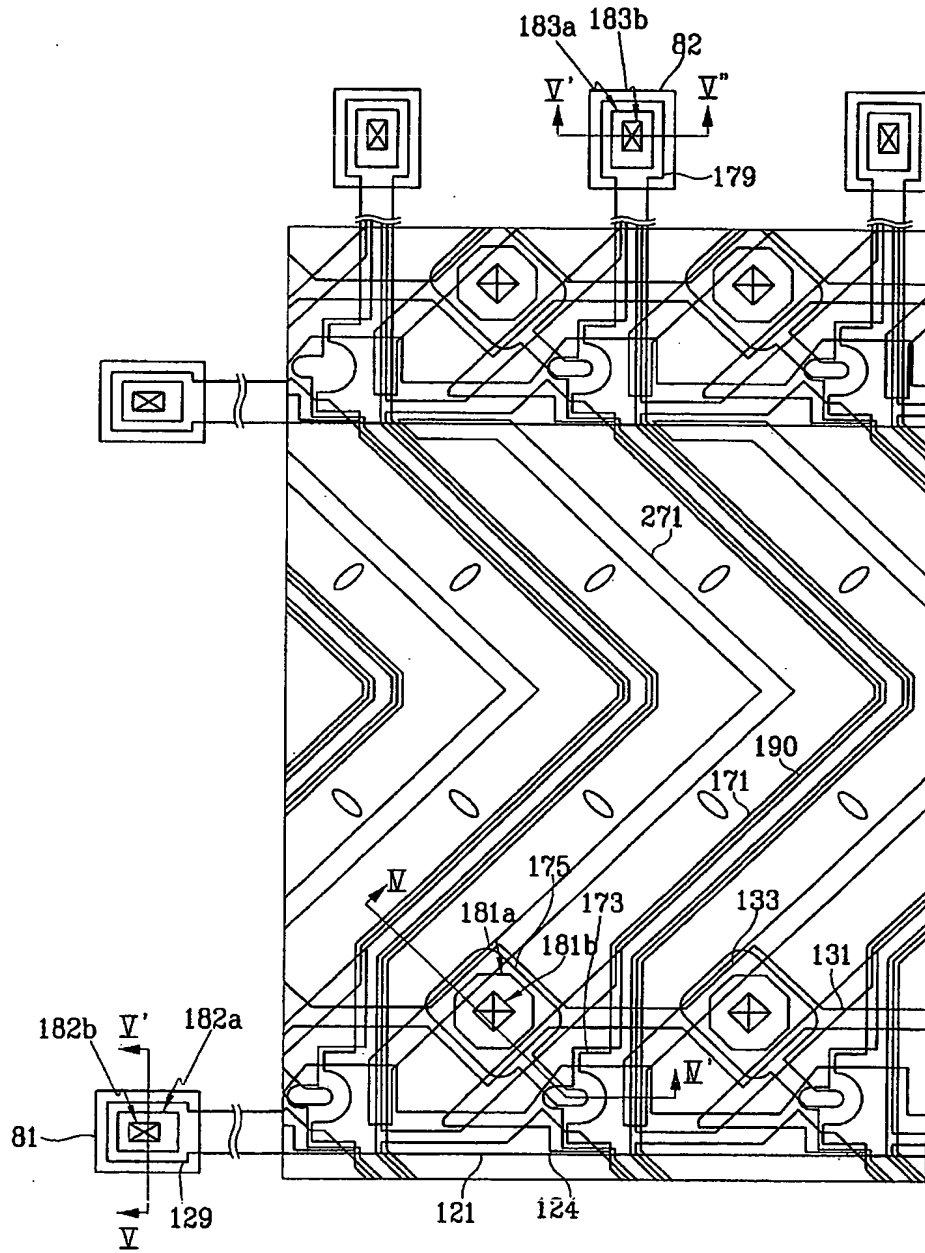


FIG.4

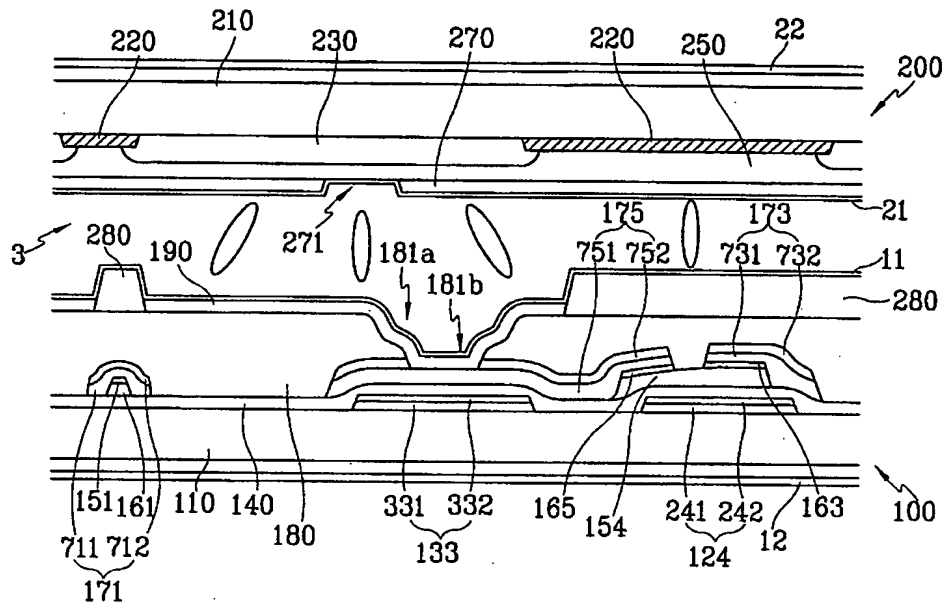


FIG.5

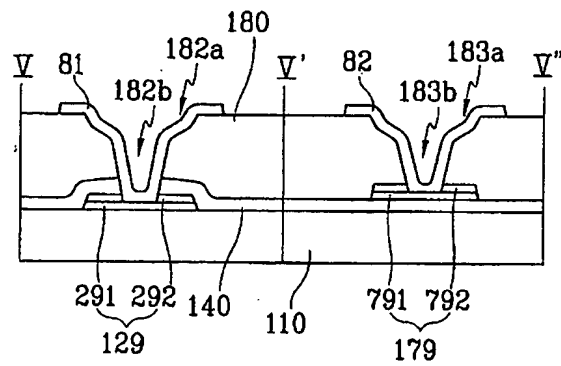


FIG.6A

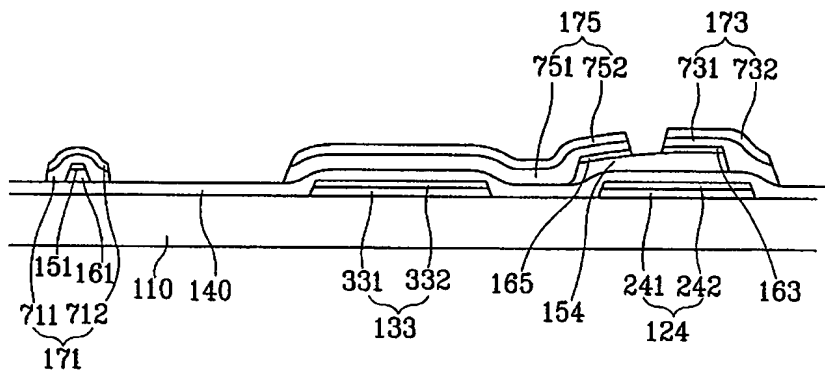
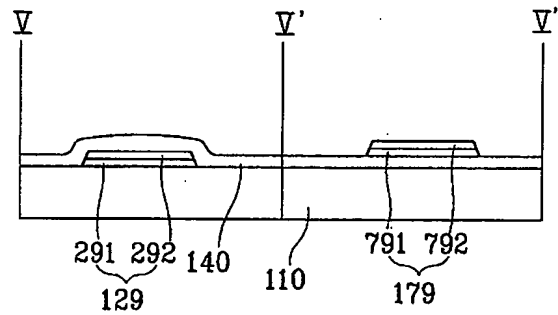


FIG.6B



[illegible]

FIG.8A

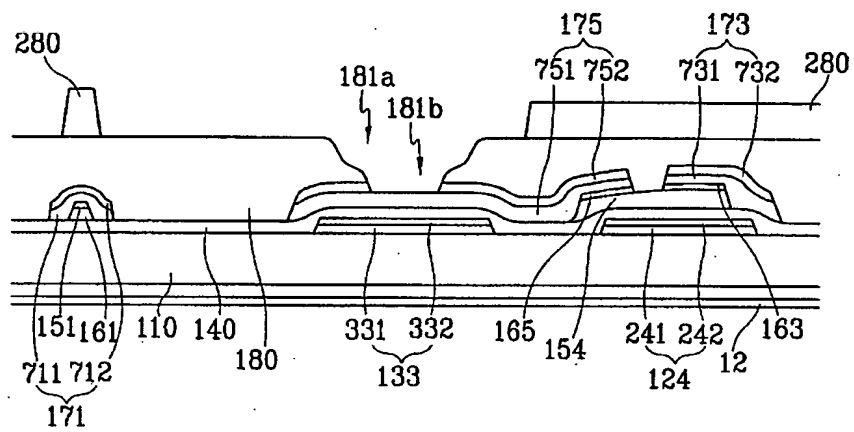


FIG.8B

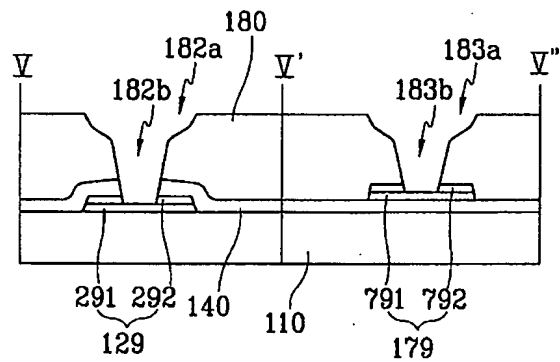
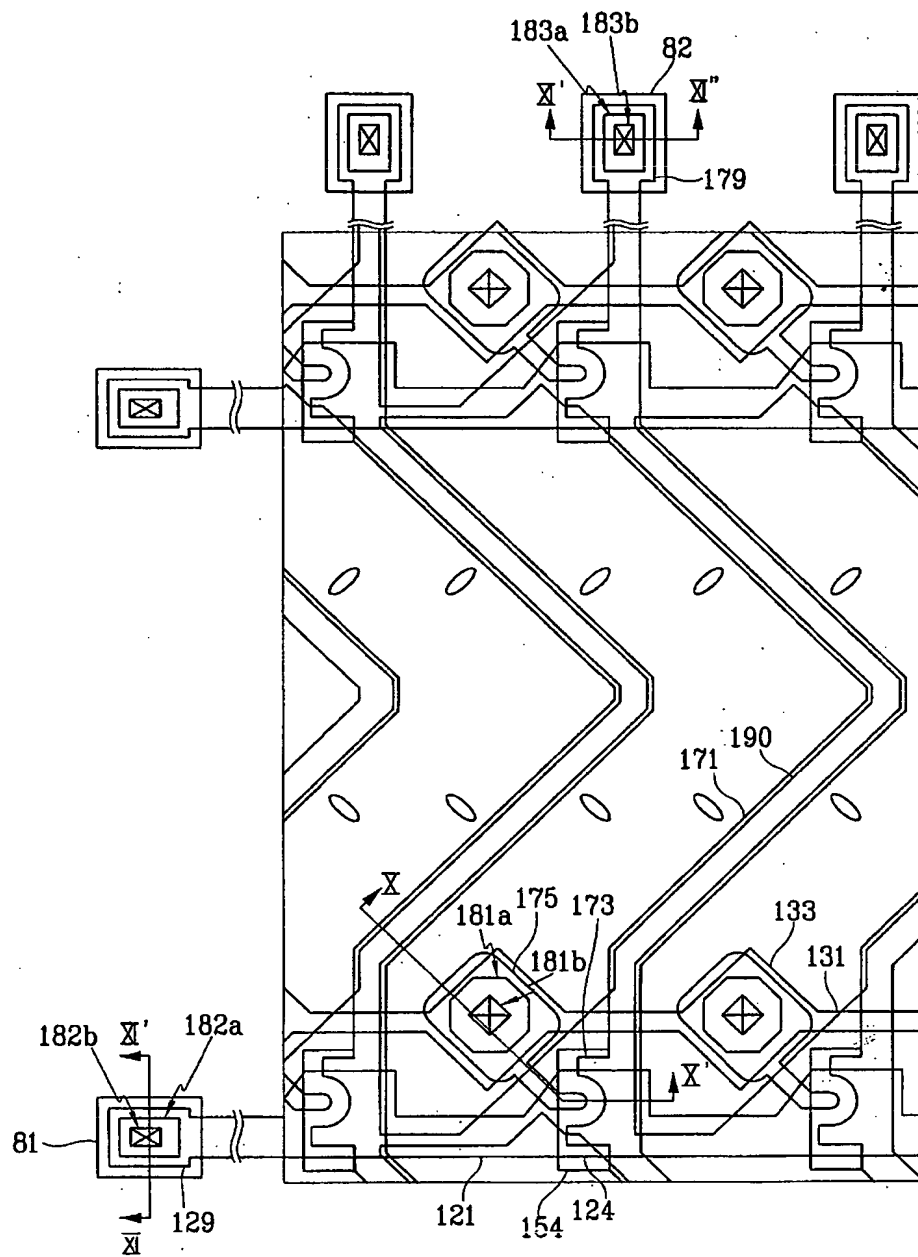


FIG.9





[illegible]

This cross-sectional view shows a semiconductor device with two gate structures. The first gate structure, on the left, consists of a gate stack 180 on a gate dielectric 140, with a gate electrode 182a and a gate electrode 182b. The second gate structure, on the right, consists of a gate stack 183a on a gate dielectric 151, with a gate electrode 183a and a gate electrode 183b. The gate stacks are separated by a channel region 110. The gate electrodes are connected to a common source/drain region 129, which is formed in a substrate 161. The source/drain region 129 is formed in a substrate 161, which is a p-type semiconductor. The source/drain region 129 is formed in a substrate 161, which is a p-type semiconductor. The source/drain region 129 is formed in a substrate 161, which is a p-type semiconductor.

FIG.12A

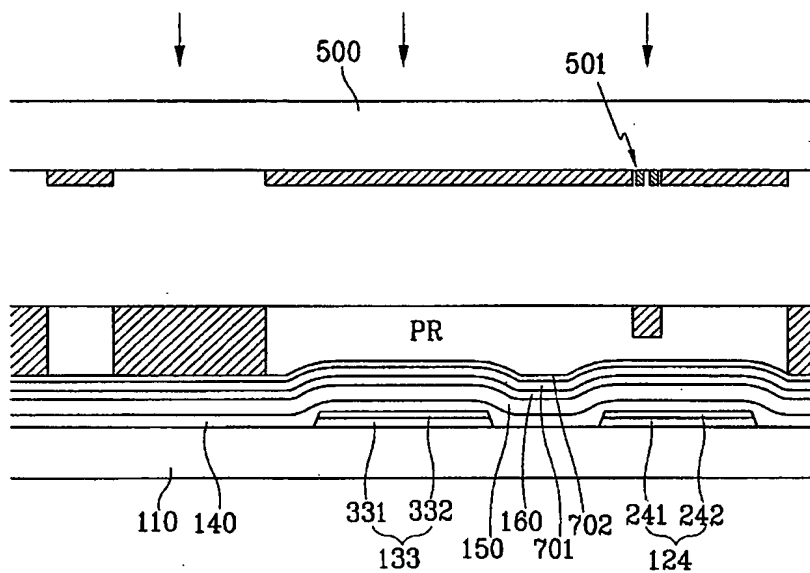


FIG.12B

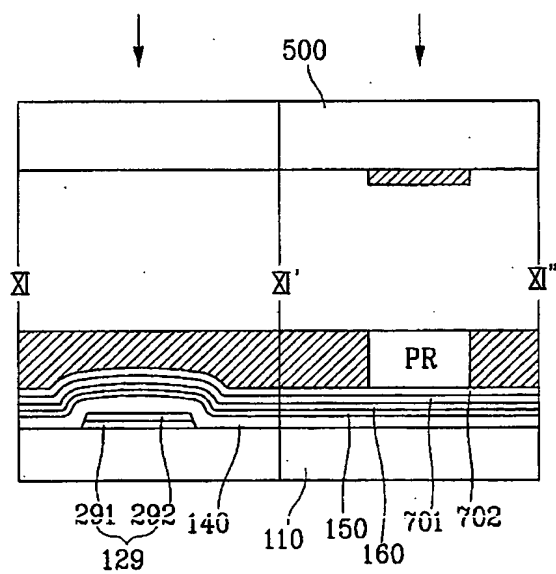


FIG.13A

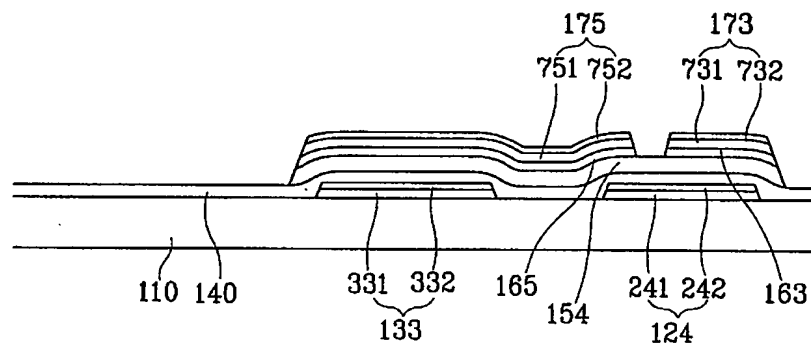


FIG.13B

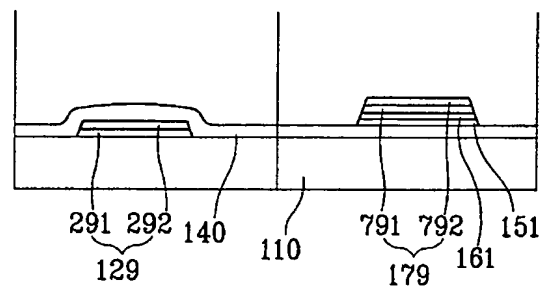


FIG.14A

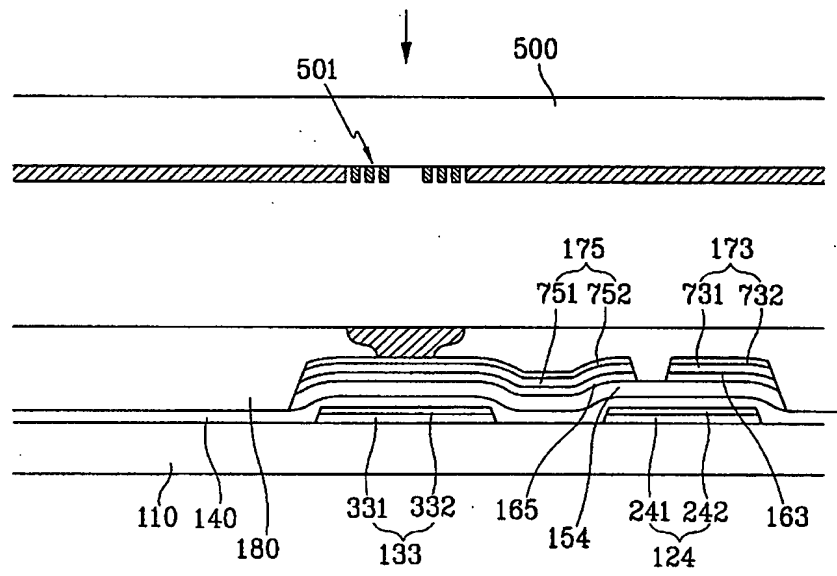
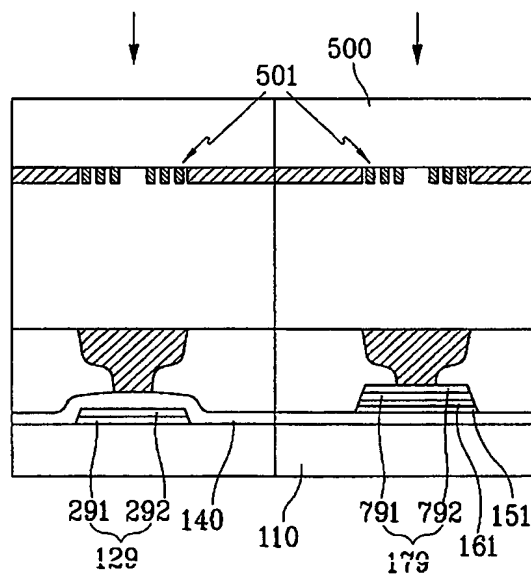


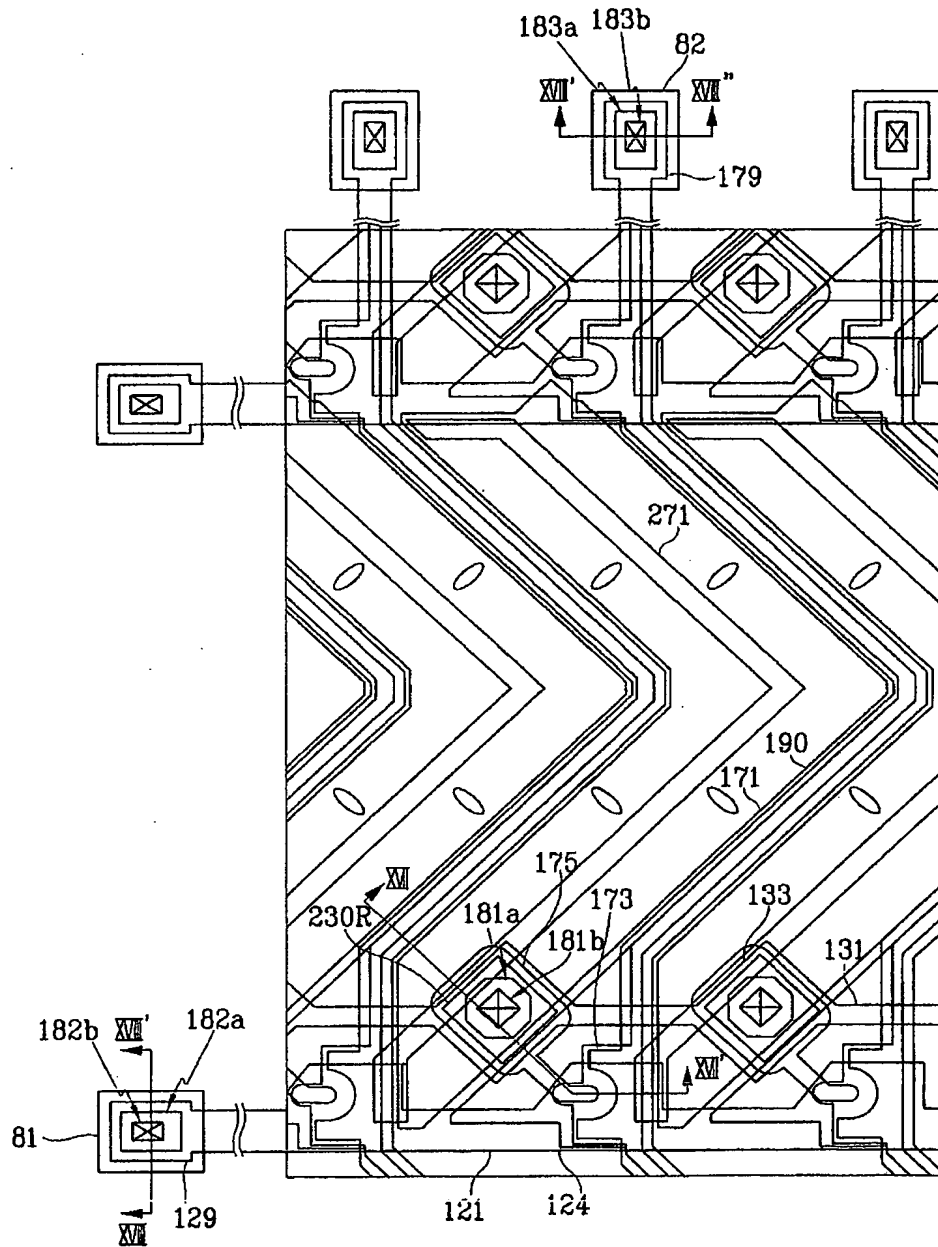
FIG.14B



This cross-sectional view shows a substrate 110 with a top layer 140 and a bottom layer 180. A series of layers 151, 161, 171, 181a, and 181b are deposited on the substrate. A patterned layer 165 is formed on top of the substrate, with a central opening 124. The opening is defined by a layer 154. The top surface of the device is covered by a layer 280. Other features include a layer 133, a layer 163, and a layer 173. The device is shown in a cross-sectional view, with the layers and features labeled with reference numerals.

This figure shows two cross-sectional views, XI and XI', of a semiconductor device. Both views show a substrate 110 with a layer 140 on top. In view XI, a contact structure 129 is formed, consisting of a base layer 291 and a top layer 292. A trench 180 is formed in the layer 140, with its side walls labeled 182a and 182b. In view XI', a different contact structure 179 is shown, consisting of layers 791, 792, and 161. A trench 180 is also present, with side walls labeled 183a and 183b. A layer 151 is shown on the surface of the substrate 110 in view XI'.

FIG.16



This cross-sectional view shows a substrate with a top surface 210 and a bottom surface 220. A thin layer 270 is on the top surface. A patterned layer 280 is on the bottom surface, with openings 190. A layer 11 is on the bottom surface. A layer 190 is on the bottom surface. A layer 175 is on the bottom surface. A layer 173 is on the bottom surface. A layer 751 is on the bottom surface. A layer 752 is on the bottom surface. A layer 731 is on the bottom surface. A layer 732 is on the bottom surface. A layer 181a is on the bottom surface. A layer 181b is on the bottom surface. A layer 151 is on the bottom surface. A layer 161 is on the bottom surface. A layer 711 is on the bottom surface. A layer 712 is on the bottom surface. A layer 171 is on the bottom surface. A layer 110 is on the bottom surface. A layer 140 is on the bottom surface. A layer 801 is on the bottom surface. A layer 802 is on the bottom surface. A layer 331 is on the bottom surface. A layer 332 is on the bottom surface. A layer 165 is on the bottom surface. A layer 154 is on the bottom surface. A layer 241 is on the bottom surface. A layer 242 is on the bottom surface. A layer 163 is on the bottom surface. A layer 230R is on the bottom surface. A layer 133 is on the bottom surface. A layer 124 is on the bottom surface. A layer 230G is on the bottom surface. A layer 230B is on the bottom surface.

This cross-sectional view shows a semiconductor device with two gate structures. The substrate 110 is divided into two regions, 129 and 179, by a central channel 140. Each region contains a gate stack 81 and 82, respectively. The gate stacks are composed of a gate oxide 801, a gate dielectric 802, and a gate electrode 803. The gate electrodes are connected to a common gate line 140. The gate structures are separated by a gate spacer 182a and 183a. The gate spacers are connected to a common gate line 140. The gate spacers are also connected to a common gate line 140. The gate spacers are also connected to a common gate line 140. The gate spacers are also connected to a common gate line 140.

FIG.19

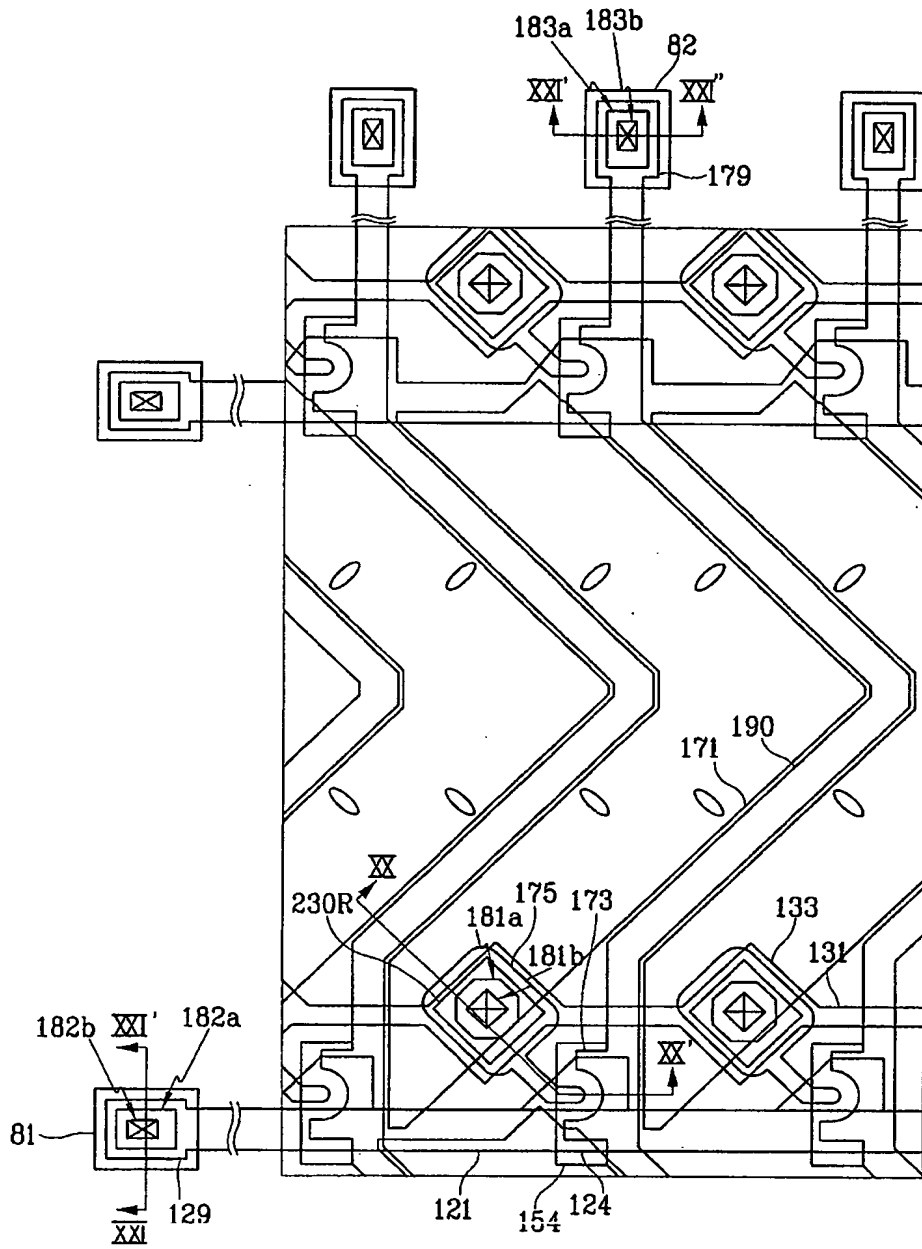




FIG.20

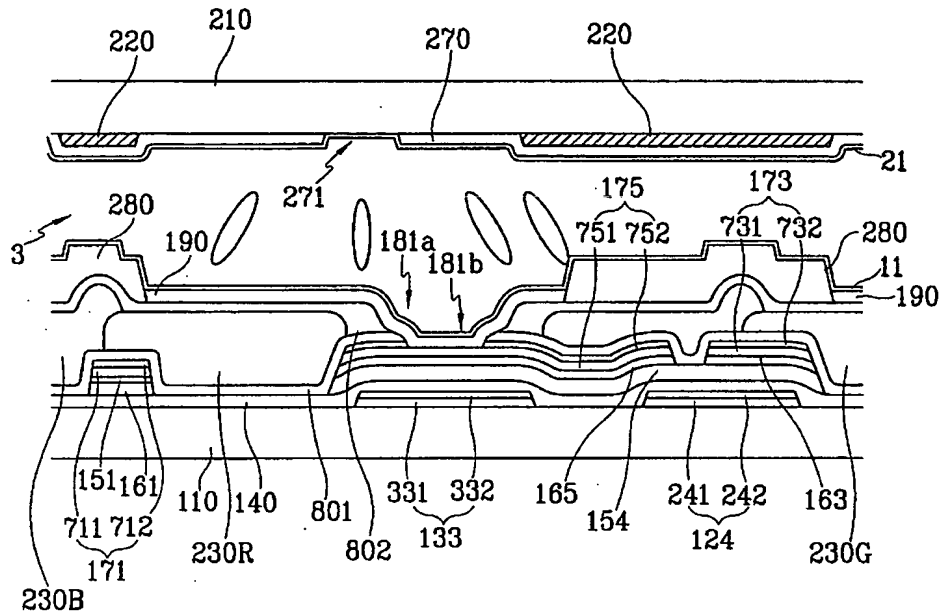


FIG.21

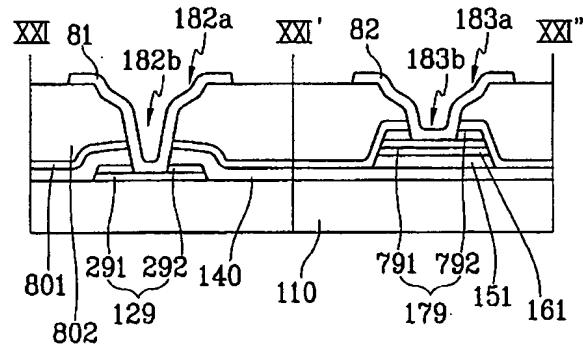


FIG.22

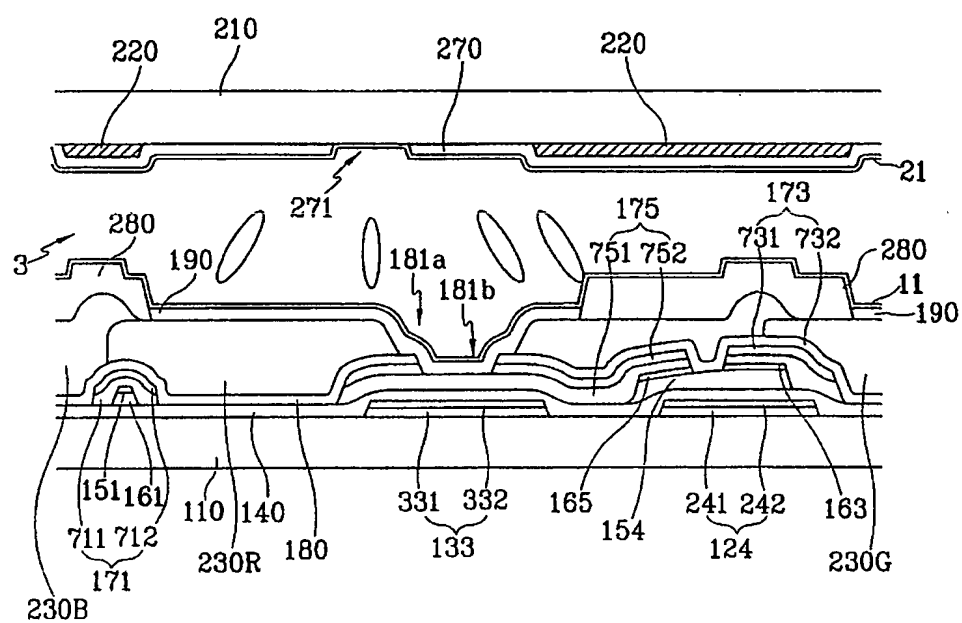


FIG.23

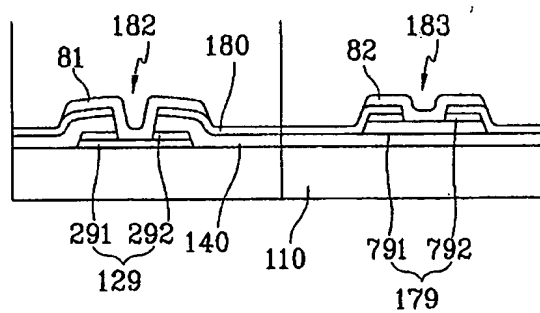


FIG.24

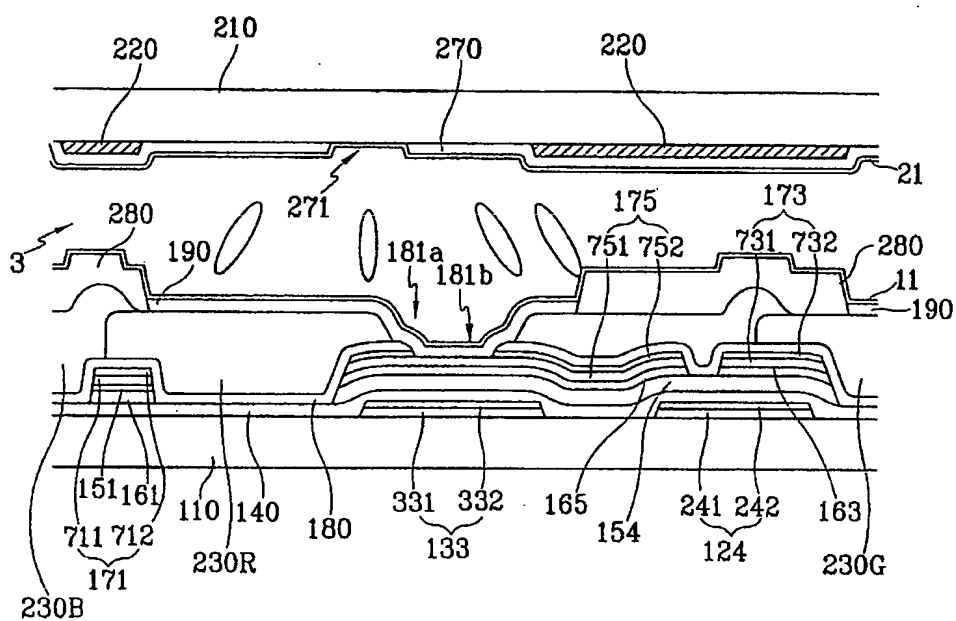
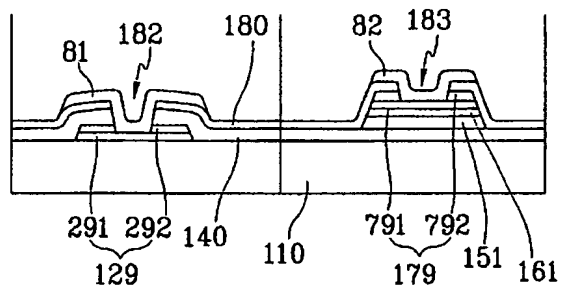


FIG.25



[illegible]

FIG.28

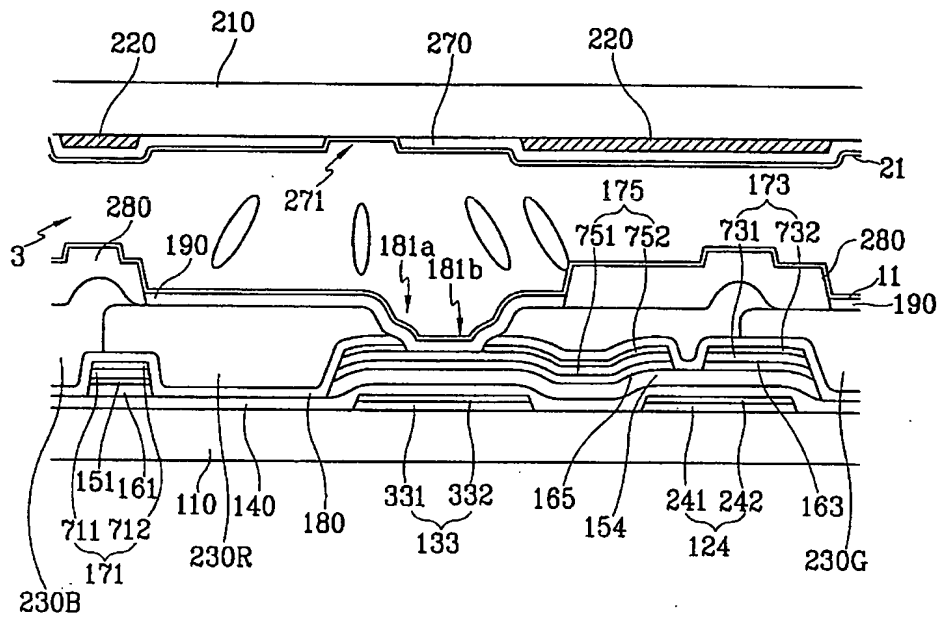


FIG.29

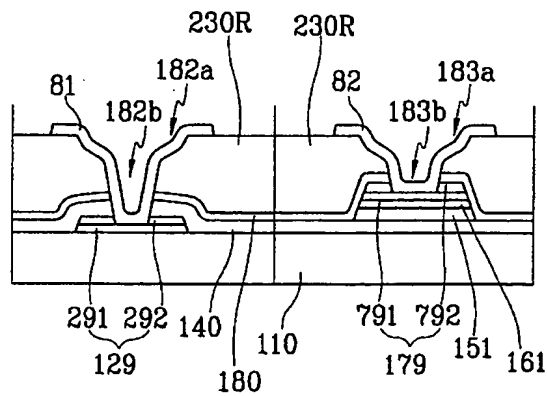


FIG.30

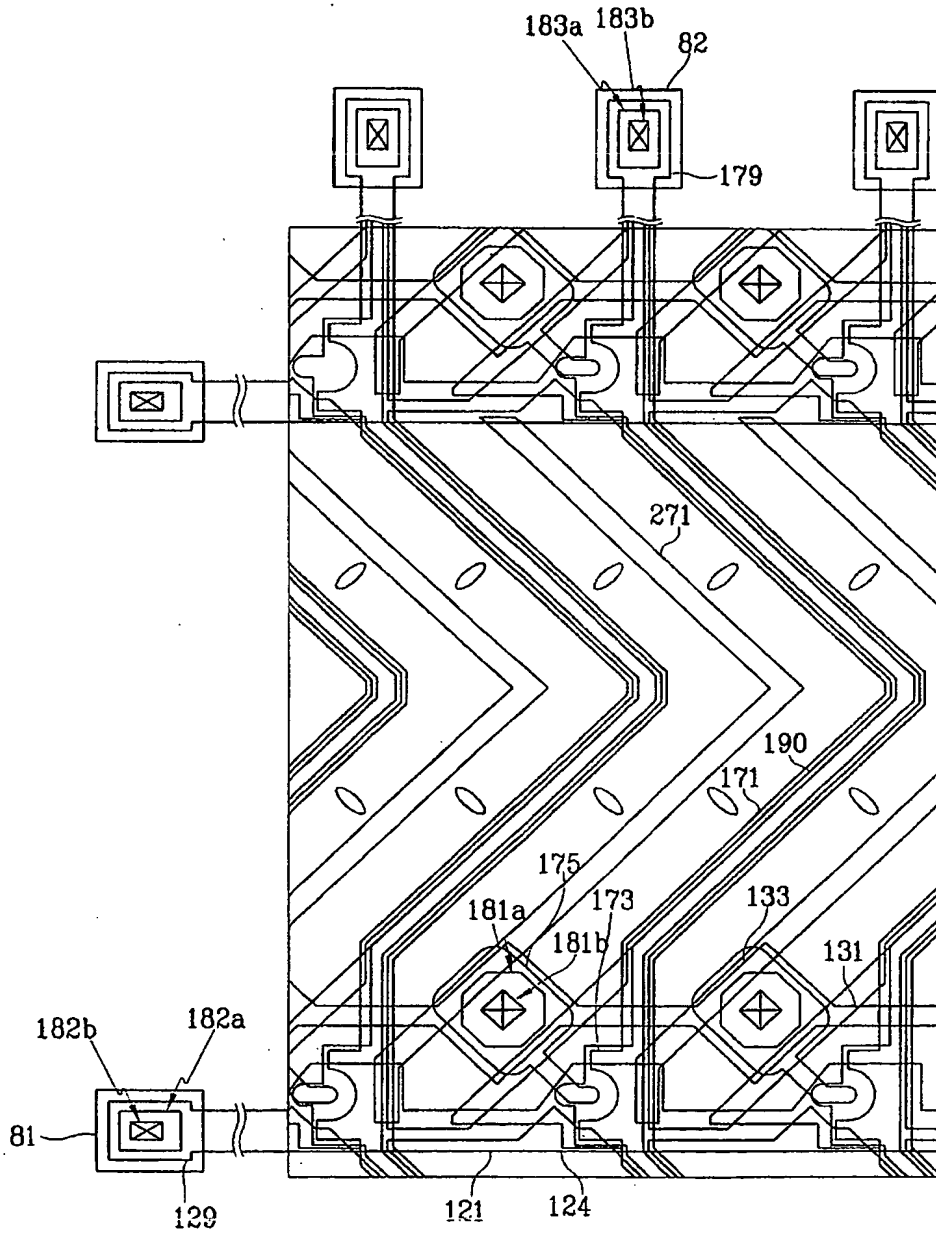


FIG.31

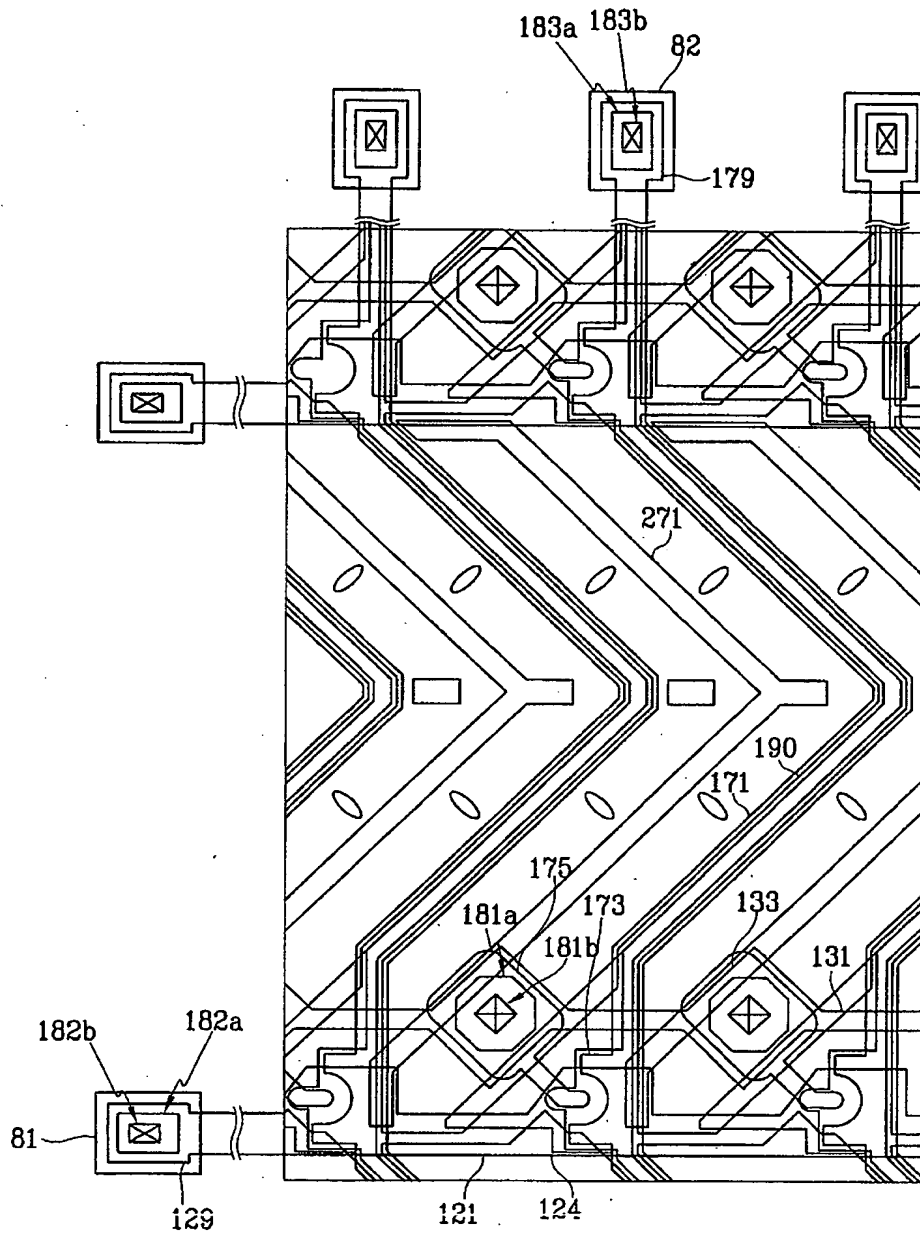


FIG.32

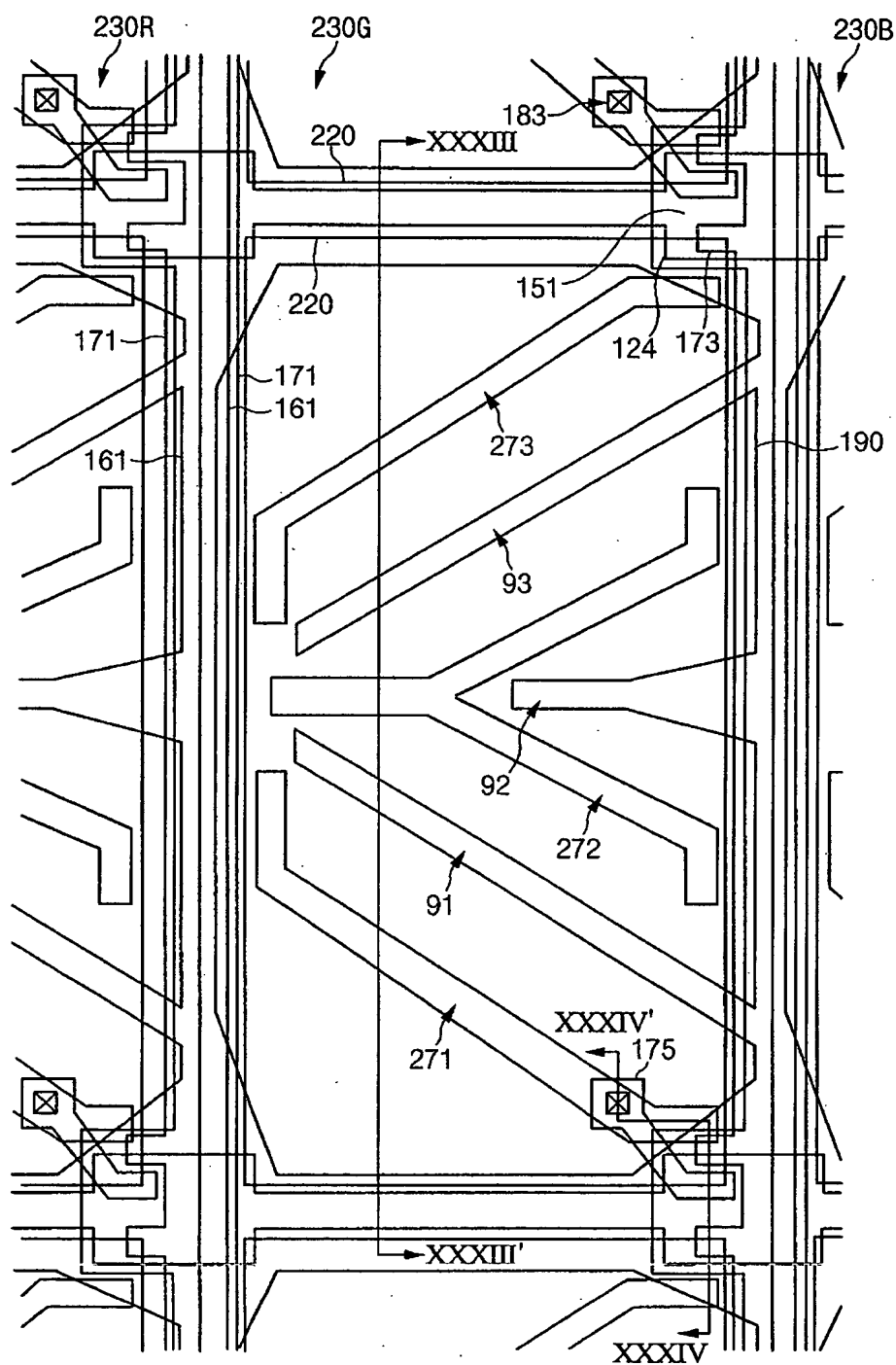




FIG.33

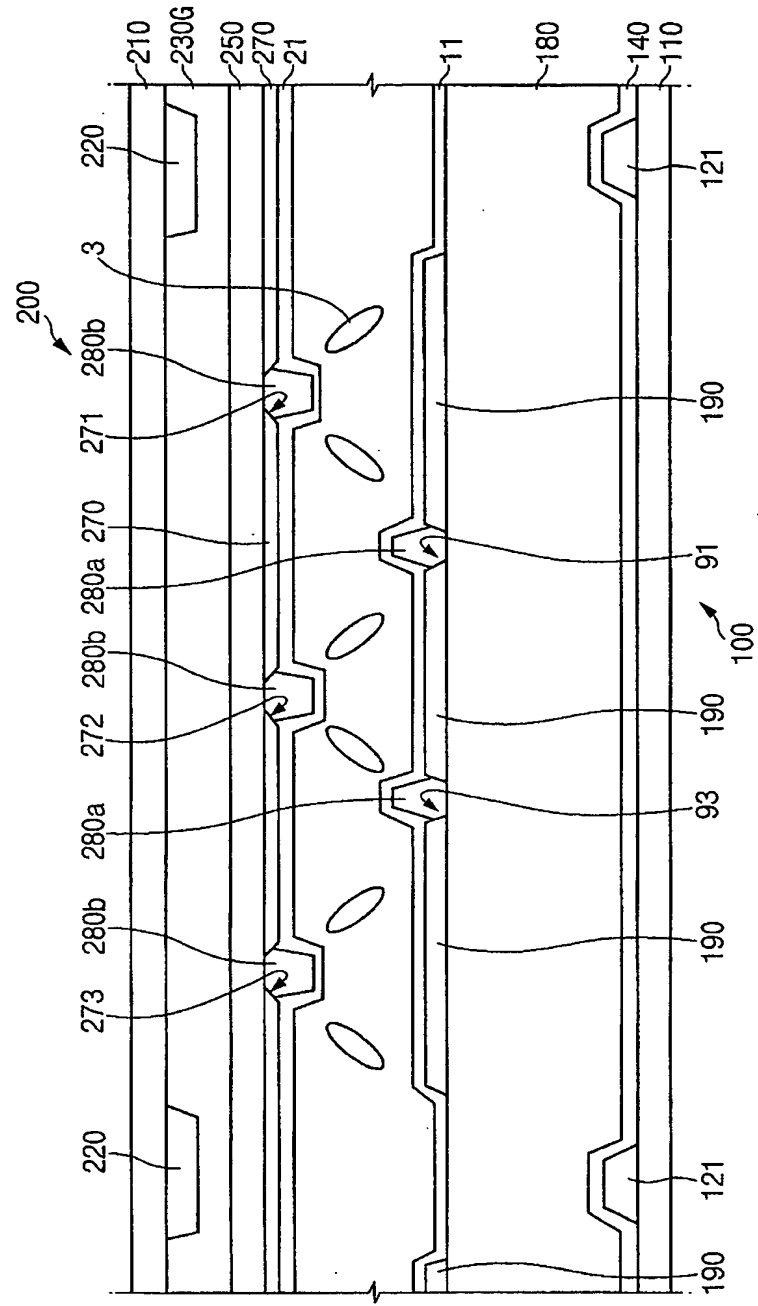


FIG.34

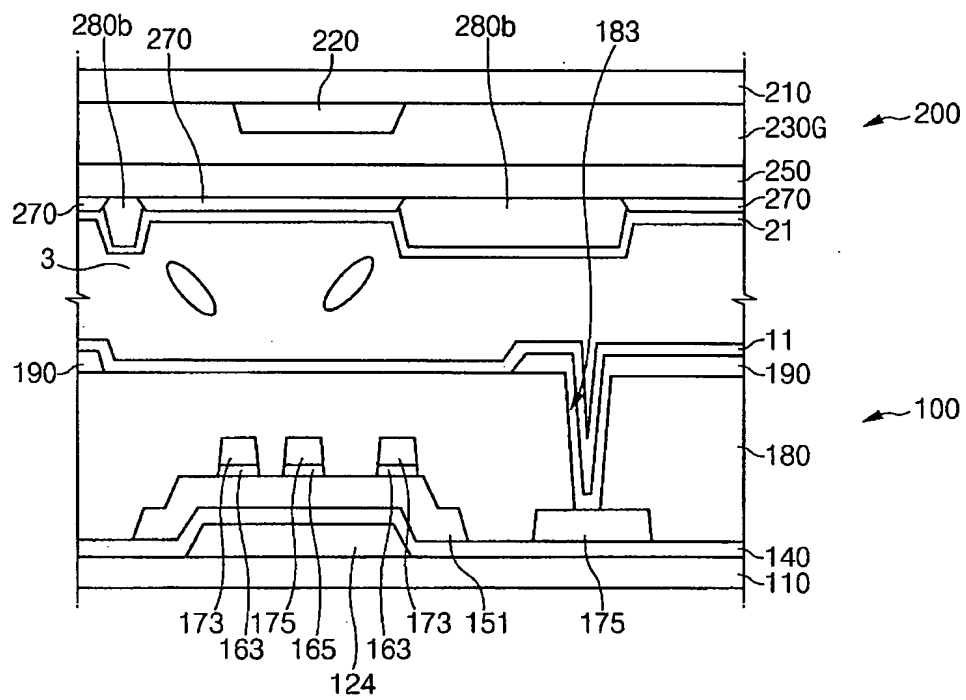


FIG.35

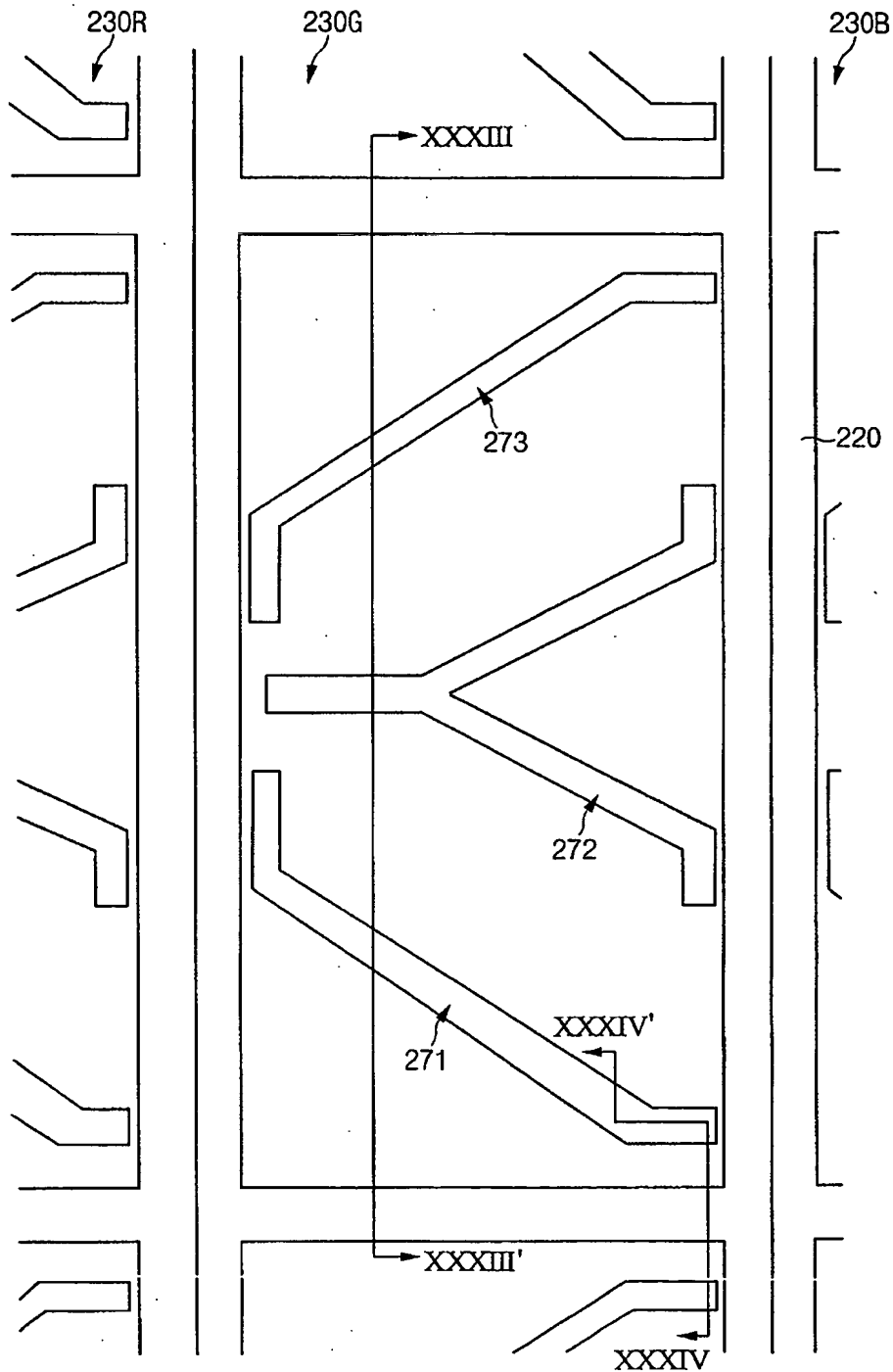


FIG.36

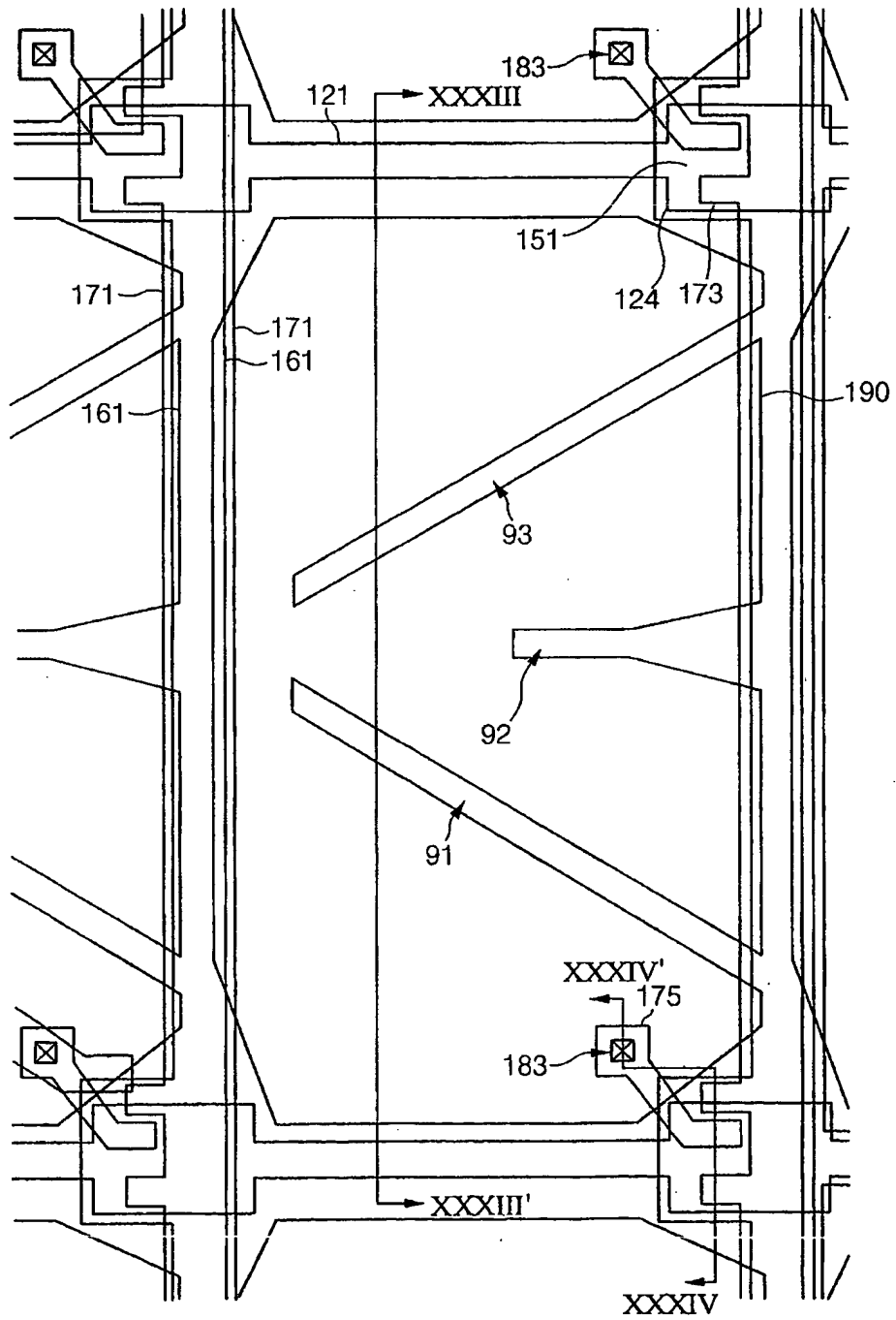


FIG.37

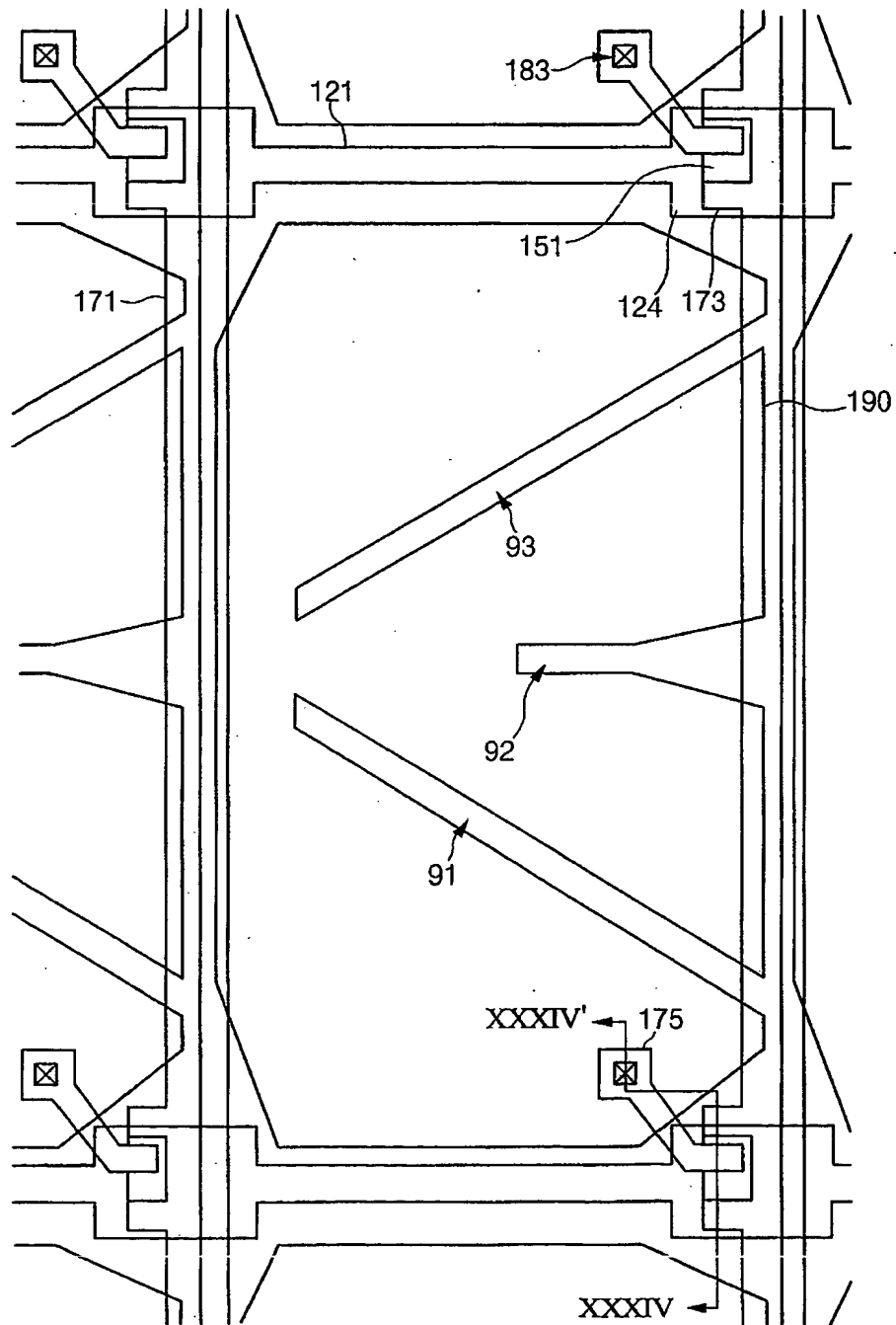


FIG.38

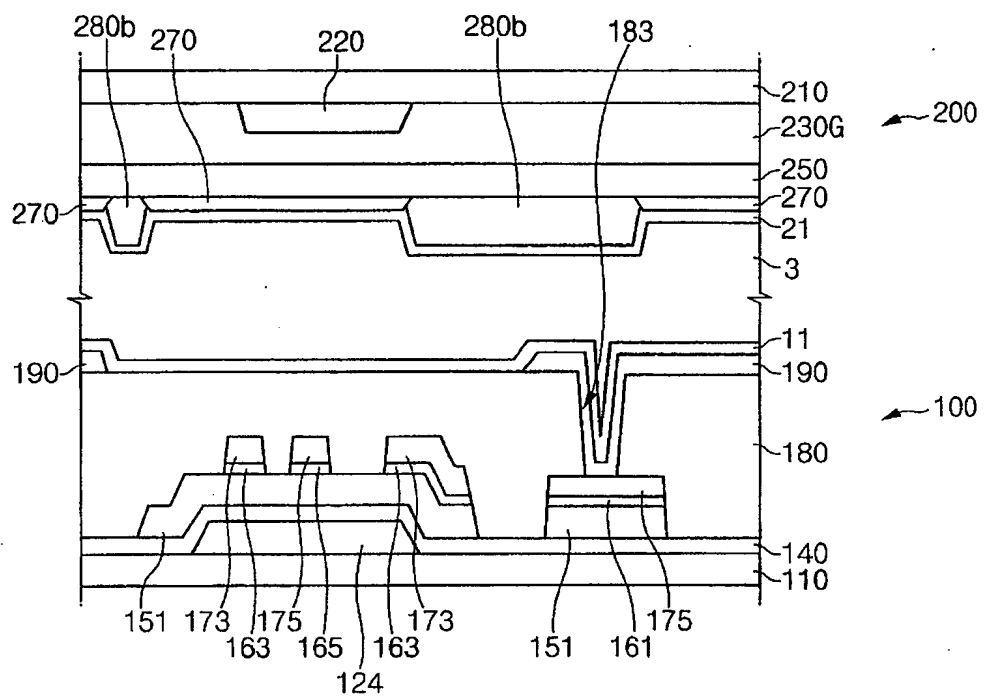


FIG.39

